Refine Search

Search Results -

Terms	Documents
L5 and @pd > 20040512	5

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Sunday, May 15, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=NO; OP=OR			
L6	L5 and @pd > 20040512	5	L6
L5	loop same invariant same range	60	L5
L4	loop same invariant same bound same range	0	L4
L3	L2 AND (upper ADJ bound)	135	L3
L2	L1 ANd range	1099	L2
L1	Loop AND invariant ANd bound	1261	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 50 of 60 returned.

☐ 1. Document ID: US 6868110 B2

L5: Entry 1 of 60 File: USPT Mar 15, 2005

US-PAT-NO: 6868110
DOCUMENT-IDENTIFIER: US 6868110 B2

TITLE: Multipath and tracking error reduction method for spread-spectrum receivers

DATE-ISSUED: March 15, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Phelts; Robert Eric	Stanford	CA		
Enge; Per	Mountain View	CA		

US-CL-CURRENT: 375/144; 370/335, 375/137, 375/149, 375/150

ABSTRACT:

A multipath mitigation method consists of locating a multipath-invariant (MPI) point of an ideal autocorrelation function and measuring the distance between the MPI point and DLL. The same MPI point is located in a received correlation function, and the distance between the point and the DLL, now affected by multipath, is measured. The difference between the ideal distance and the actual distance is the code tracking error resulting from multipath. The error is subtracted from the computed pseudorange or used to control the DLL. The method can be used to reduce the effects of all types of tracking error sources, such as signal transmission failure or code noise.

45 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KMC | Draw D

☐ 2. Document ID: US 6853164 B1

L5: Entry 2 of 60 File: USPT Feb 8, 2005

US-PAT-NO: 6853164
DOCUMENT-IDENTIFIER: US 6853164 B1

TITLE: Bandgap reference circuit

DATE-ISSUED: February 8, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Prinz; Francois X.	San Jose	CA		
Aioanei; Ovidiu	San Jose	CA		

US-CL-CURRENT: 320/119; 320/121

ABSTRACT:

A bandgap reference circuit and method of using the same are provided. The bandgap reference circuit may provide start-up requirements at substantially any voltage and at substantially any temperature. The circuit comprises an op amp (two stages of transistors) and a network of resistors and bipolar diodes. When an artificial offset of about -5 mV is introduced to the op amp, the op amp output will be high as soon as the power supply exceeds the transistors' threshold voltages. The op amp output supplies the resistor and diode network and brings the op amp inputs within desired regulation voltages.

16 Claims, 7 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

☐ 3. Document ID: US 6795780 B1

L5: Entry 3 of 60 File: USPT Sep 21, 2004

US-PAT-NO: 6795780
DOCUMENT-IDENTIFIER: US 6795780 B1

TITLE: Fluid energy pulse test system--transient, ramp, steady state tests

DATE-ISSUED: September 21, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hyde; Thomas Allen	Midland	TX	79701-4031	

US-CL-CURRENT: 702/45; 700/281, 702/46, 702/47, 702/50, 702/51, 73/61.56

ABSTRACT:

In improvements to the Fluid Energy Pulse Test System, apparatus and methods regulate high-pressure, high-fluid-flow-rate energy pulses to generate temperature-controlled transient, ramp, constant-steady-state, and periodic-steady-state fluid-pressure and fluid-flow-rate test data and sound data for evaluating fluid control devices. Transient, ramp, and constant-steady-state performance curves describe

dynamic operating characteristics of tested devices. Transient and constant-steady-state pressures and flow rates are precisely defined and compared. Constant fluid conductance is represented by transverse lines on performance graphs. Constant- and periodic-steady-state pressures and flow rates are achieved in less than two seconds. Temperature sensitivity of fluid control devices is determined. Fluid-pressure and fluid-flow-rate data correlated with sound data create audio-visual representations. Three-dimensional amplitude-frequency-time sound signatures are displayed graphically.

30 Claims, 40 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

☐ 4. Document ID: US 6772414 B1

L5: Entry 4 of 60 File: USPT Aug 3, 2004

US-PAT-NO: 6772414
DOCUMENT-IDENTIFIER: US 6772414 B1

TITLE: Lifetime-sensitive mechanism and method for hoisting invariant computations out of loops in a computer program

DATE-ISSUED: August 3, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Roediger; Robert Ralph	Rochester	MN		
Schmidt; William Jon	Rochester	MN		

US-CL-CURRENT: 717/160; 717/150, 717/156

ABSTRACT:

A mechanism and method for hoisting invariant computations from loops analyzes the lifetimes of fixed processor resources defined by an instruction, and determines whether a group of computations present in multiple instructions within the lifetime are, taken together, loop-invariant and legal to hoist from the loop. If the group of computations within the lifetime of the fixed processor resource are loop-invariant and hoistable, all of the computations are hoisted out of the loop as a group. By determining the lifetimes of fixed processor resources defined in an instruction, the hoisting mechanism succeeds in hoisting out groups of computations that cannot be individually hoisted out of a loop, thereby achieving better performance when the computer program executes.

15 Claims, 13 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 5. Document ID: US 6766239 B2

L5: Entry 5 of 60 File: USPT Jul 20, 2004

US-PAT-NO: 6766239
DOCUMENT-IDENTIFIER: US 6766239 B2

TITLE: Advanced wheel slip detection using suspension system information

DATE-ISSUED: July 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Barron; Richard J.	Ann Arbor	MI		
Milot; Danny R.	Ann Arbor	MI		

US-CL-CURRENT: 701/71; 180/197, 303/139, 701/70, 701/79, 701/82, 701/91

ABSTRACT:

The present invention determines a longitudinal wheel speed of an individual wheel from an angular rate signal from a wheel rotation sensor. Vehicle suspension information or operating characteristics are input to a suspension system mathematical model to determine instantaneous rolling radius, taking into account changes in tire rolling radius resulting from vertical motion of the road surface. Improved accuracy of wheel speed permits less severe filtering of wheel speeds in detecting wheel slip and/or modified speed and acceleration thresholds in slip control.

16 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

☐ 6. Document ID: US 6724329 B2

L5: Entry 6 of 60 File: USPT Apr 20, 2004

US-PAT-NO: 6724329
DOCUMENT-IDENTIFIER: US 6724329 B2
**** See image for Certificate of Correction ****

TITLE: Decision feedback equalization employing a lookup table

DATE-ISSUED: April 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Casper; Bryan K.	Hillsboro	OR		

US-CL-CURRENT: 341/106; 341/118, 341/120, 341/123, 341/155

ABSTRACT:

A decision feedback equalizer includes a lookup table device. The lookup table device may include a shift register and memory, or may include multiple shift registers and memories. Near-end crosstalk may be reduced using a lookup table device. Echo in a bi-directional port circuit may also be reduced using a lookup table device.

20 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

☐ 7. Document ID: US 6665864 B1

L5: Entry 7 of 60 File: USPT Dec 16, 2003

US-PAT-NO: 6665864
DOCUMENT-IDENTIFIER: US 6665864 B1

TITLE: Method and apparatus for generating code for array range check and method and apparatus for versioning

DATE-ISSUED: December 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kawahito; Motohiro	Sagamihara			JP
Komatsu; Hideaki	Yokohama			JP
Yasue; Toshiaki	Sagamihara			JP

US-CL-CURRENT: 717/151; 717/122, 717/152, 717/160

ABSTRACT:

The present invention eliminates redundant array range checks. A two-phased check is performed, namely a wide range check is performed by combining a plurality of array range checks, and a strict range check is unsuccessful, so as to reduce the number of range checks at execution time and allow execution at high speed. For instance, it is possible with a processor such as PowerPC, by using a flag, to invalidate a code for performing an array range check at high speed without increasing a code size. Consequently, the number of array range checks to be executed can be reduced so as to allow execution at high speed. Also, for instance, a plurality of array range checks can be combined without considering existence of instructions which cause a side effect. Consequently, the number of array range checks to be executed can be reduced so as to allow execution at high speed. In addition, a versioning is performed by using, as array access information for versioning, information of array access information for versioning information of array accesses which are always performed even if passing through any execution path in a loop so that there are fewer cases where it goes to a version with a larger number of array range checks at execution time.

18 Claims, 15 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 8. Document ID: US 6614296 B2

L5: Entry 8 of 60 File: USPT Sep 2, 2003

US-PAT-NO: 6614296
DOCUMENT-IDENTIFIER: US 6614296 B2

TITLE: Equalization of a transmission line signal using a variable offset comparator

DATE-ISSUED: September 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Casper; Bryan K.	Hillsboro	OR		

US-CL-CURRENT: 330/9; 327/307, 330/252, 330/258, 330/259, 703/1, 703/13

ABSTRACT:

According to an embodiment, an equalization loop has a comparator with an input to receive a transmission line analog signal level. The comparator has a substantially variable offset that is controllable to represent a variable reference level. An output of the comparator provides a value that represents a comparison between the transmission line analog signal level and the variable reference level.

19 Claims, 9 Drawing figures
Exemplary Claim Number: 8
Number of Drawing Sheets: 8

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 9. Document ID: US 6556509 B1

L5: Entry 9 of 60 File: USPT Apr 29, 2003

US-PAT-NO: 6556509
DOCUMENT-IDENTIFIER: US 6556509 B1

TITLE: Demodulator and method for interferometric outputs of increased accuracy

DATE-ISSUED: April 29, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cekorich; Allen Curtis	Walnut Creek	CA		
Davis; Joseph Grau	Lafayette	CA		

US-CL-CURRENT: 356/477; 356/460

ABSTRACT:

An apparatus and method is presented to provide wide dynamic range balanced measurements of the input phase to an interferometer using a phase generated carrier especially useful utilizing time multiplexing to demodulate a series of interferometers with high accuracy. A modulation drive output is provided by the invention and maintained under operation at the optimum amplitude by an internal feedback loop. The resulting highly stable system which is time balanced, can be fabricated from an analog to digital converter, a digital signal processor, and a digital to analog converter making low cost open loop demodulators a reality.

27 Claims, 41 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

☐ 10. Document ID: US 6505778 B1

L5: Entry 10 of 60 File: USPT Jan 14, 2003

US-PAT-NO: 6505778
DOCUMENT-IDENTIFIER: US 6505778 B1
**** See image for Certificate of Correction ****

TITLE: Optical reader with selectable processing characteristics for reading data in multiple formats

DATE-ISSUED: January 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reddersen; Brad R.	Eugene	OR		
Bremer; Edward C.	Rochester	NY		
La; Chay K.	Rochester	NY		
Deloge; Stephen P.	Rochester	NY		
Boyd; Raymond J.	Bloomfield	NY		
Cooper; Shane P.	Walworth	NY		
Zaverukha; Ilya	Penfield	NY		

US-CL-CURRENT: 235/462.25; 235/462.26

ABSTRACT:

A multi-function optical reader comprises an photosensor, such as a charge-device

(CCD), and signal conditioning and processing circuitry including separate channels for handling data in different formats. A bar code processing channel digitizes the scan signal according to light and dark features using a first-derivative technique, and an OMR processing channel uses an adaptive threshold to adapt to different light conditions and provide a boundary line for digitizing light and dark features of the target scan line. A feature measurement circuit measures the widths of the light and dark regions as derived by the separate processing channels, and provides the feature measurements to a decoding system or host terminal processor. The scan rate of the optical reader can be adjusted according to the data format to be read or the level of ambient light, to avoid saturation. The optical reader can provide multiple depth-of-field zones, both internal and external to an optical reader housing. The optical reader may provide for image capture and optical character recognition.

22 Claims, 49 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 38

☐ 11. Document ID: US 6461604 B1

L5: Entry 11 of 60 File: USPT Oct 8, 2002

US-PAT-NO: 6461604
DOCUMENT-IDENTIFIER: US 6461604 B1

TITLE: Crystalline IL-6 and models of the molecular structure of IL-6

DATE-ISSUED: October 8, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Somers; William S.	Boston	MA		
Stahl; Mark L.	Wilmington	MA		
Seehra; Jasbir S.	Lexington	MA		
Xu; Guang-Yi	Arlington	MA		
McDonagh; Thomas E.	Acton	MA		
Yu; Hsiang-Ai	Andover	MA		
Hong; Jin	Ayer	MA		

US-CL-CURRENT: 424/85.2; 435/69.52, 530/351, 530/402, 530/412, 530/418, 530/419, 530/420

ABSTRACT:

Crystallographic and NMR solution structures of human IL-6 are reported. The invention provides models and systems incorporating such structures which are useful for identifying IL-6/IL-6 receptor interactions and for identification of agonists and antagonists of such interactions. Crystalline human IL-6 is also provided.

14 Claims, 18 Drawing figures

Exemplary Claim Number: 1
Number of Drawing Sheets: 15

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 12. Document ID: US 6392547 B1

L5: Entry 12 of 60 File: USPT May 21, 2002

US-PAT-NO: 6392547
DOCUMENT-IDENTIFIER: US 6392547 B1

TITLE: Proximity monitoring system and associated methods

DATE-ISSUED: May 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stewart; Art	Melbourne Beach	FL		
Olaker; David Allen	Melbourne	FL		

US-CL-CURRENT: 340/573.1; 340/551, 340/825.36

ABSTRACT:

A proximity detection system includes a magnetic field generator for generating a rotating magnetic field having a decreasing intensity over an increasing separation distance, and a magnetic field detector being relatively movable and generating a crossing indication based upon an intensity threshold in the rotating magnetic field being crossed as a threshold separation distance from the magnetic field generator is crossed. The system may also include a transmitter for transmitting a signal relating to the crossing indication from the magnetic field detector. The magnetic field generator may generate a substantially constant amplitude rotating magnetic field vector, and the magnetic field detector may comprise a plurality of orthogonal detection coils. The rotating magnetic field provides a relatively sharp cut-off threshold separation distance defining a perimeter for proximity detection.

46 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 13. Document ID: US 6366591 B1

L5: Entry 13 of 60 File: USPT Apr 2, 2002

US-PAT-NO: 6366591
DOCUMENT-IDENTIFIER: US 6366591 B1

TITLE: Technique for treating channel impairments involving measuring a digital

loss in transmitted signals in data communications

DATE-ISSUED: April 2, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lai; Yhean-Sen	Warren	NJ		

US-CL-CURRENT: 370/523

ABSTRACT:

In a communications arrangement, a first pulse code modulation (PCM) modem communicates data in the form of PCM words with a second PCM modem through a public switched telephone network (PSTN). Transmitted signals representing PCM words may be affected by robbed bit signaling occasioned by the PSTN such that the least significant bits (LSBs) of certain transmitted PCM words are "robbed" and substituted with signaling bits. In addition, the transmitted signals are attenuated because of a digital loss imposed by a switch in the PSTN. During training of a PCM modem, any occurrence of robbed bit signaling is identified, and a signal level conversion table is created. This table contains each transmitted PCM word and the received signal level corresponding thereto. In accordance with the invention, the digital loss is measured based on those received signal levels in the table which are free of robbed bit signaling.

35 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

☐ 14. Document ID: US 6311895 B1

L5: Entry 14 of 60 File: USPT Nov 6, 2001

US-PAT-NO: 6311895
DOCUMENT-IDENTIFIER: US 6311895 B1

TITLE: Optical reader with condensed CMOS circuitry

DATE-ISSUED: November 6, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olmstead; Bryan L.	Eugene	OR		
Colley; James E.	Eugene	OR		

US-CL-CURRENT: 235/462.41; 235/454, 235/470

ABSTRACT:

An optical or symbol reader including CMOS circuitry preferably integrated on a

single chip. A CMOS optical reader chip comprises a CMOS imaging array having a plurality of pixels each with a dedicated pixel-site circuit. Charge is accumulated at each pixel location transferred upon demand to a common bus. In a preferred embodiment, exposure time of the imaging array is controlled using a feedback loop. One or more exposure control pixels are positioned adjacent to or within the imaging array and receive light along with the imaging array. The charge of the exposure control pixel or pixels is measured against a threshold level, and the amount of time taken to reach the threshold level determines the time exposure of the pixels of the imaging array. CMOS signal processing circuitry is employed which, in combination with the exposure control circuitry, minimizes time-to-read over a large range of light levels, while performing spatially optimal filtering. Clocking cycles and control signals are time-adjusted in accordance with the varying output frequency of the imaging array so as to provide invariant frequency response by the signal processing circuitry. A multi-dimensional CMOS imaging array is also provided having simultaneous pixel exposure with non-destructive readout of the pixel contents.

28 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 11

☐ 15. Document ID: US 6301706 B1

L5: Entry 15 of 60 File: USPT Oct 9, 2001

US-PAT-NO: 6301706
DOCUMENT-IDENTIFIER: US 6301706 B1

TITLE: Compiler method and apparatus for elimination of redundant speculative computations from innermost loops

DATE-ISSUED: October 9, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maslennikov; Dmitry M.	Moscow			RU
Volkonsky; Vladimir Y.	Moscow			RU

US-CL-CURRENT: 717/160; 712/24, 712/241

ABSTRACT:

A method and system for use with VLIW processing architectures for avoiding redundant speculative computations in the compilation of the innermost loops. The method includes identifying a plurality of compiled flow paths, where each of the paths includes a plurality of conditions associated with the loop that permits transformation of the loop for more optimum execution. It is then determined whether the loop has an inductive variable and a conditional statement that depends on the inductive variable. It is also determined whether the loop set up values of the inductive variables to subsets, and at least one of which the conditional statement is a loop invariant. Finally, if conditions in the determination steps satisfy the conditions of one of the paths, the loop is transformed into two

consecutive loops executable with a reduced set of values of the inductive variable.

6 Claims, 1 Drawing figures
Exemplary Claim Number: 6
Number of Drawing Sheets: 1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 16. Document ID: US 6276605 B1

L5: Entry 16 of 60 File: USPT Aug 21, 2001

US-PAT-NO: 6276605
DOCUMENT-IDENTIFIER: US 6276605 B1

TITLE: Optical reader with condensed CMOS circuitry

DATE-ISSUED: August 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olmstead; Bryan L.	Eugene	OR		
Colley; James E.	Eugene	OR		

US-CL-CURRENT: 235/462.41; 235/454, 235/470

ABSTRACT:

An optical or symbol reader including CMOS circuitry preferably integrated on a single chip. A CMOS optical reader chip comprises a CMOS imaging array having a plurality of pixels each with a dedicated pixel-site circuit. Charge is accumulated at each pixel location transferred upon demand to a common bus. In a preferred embodiment, exposure time of the imaging array is controlled using a feedback loop. One or more exposure control pixels are positioned adjacent to or within the imaging array and receive light along with the imaging array. The charge of the exposure control pixel or pixels is measured against a threshold level, and the amount of time taken to reach the threshold level determines the time exposure of the pixels of the imaging array. CMOS signal processing circuitry is employed which, in combination with the exposure control circuitry, minimizes time-to-read over a large range of light levels, while performing spatially optimal filtering. Clocking cycles and control signals are time-adjusted in accordance with the varying output frequency of the imaging array so as to provide invariant frequency response by the signal processing circuitry. A multi-dimensional CMOS imaging array is also provided having simultaneous pixel exposure with non-destructive readout of the pixel contents.

20 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 17. Document ID: US 6230975 B1

L5: Entry 17 of 60 File: USPT May 15, 2001

US-PAT-NO: 6230975
DOCUMENT-IDENTIFIER: US 6230975 B1

TITLE: Optical reader with adaptive exposure control

DATE-ISSUED: May 15, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Colley; James E.	Eugene	OR		
Olmstead; Bryan L.	Eugene	OR		

US-CL-CURRENT: 235/462.06; 235/462.25

ABSTRACT:

An optical or symbol reader including CMOS circuitry preferably integrated on a single chip. A CMOS optical reader chip comprises a CMOS imaging array having a plurality of pixels each with a dedicated pixel-site circuit. Charge is accumulated at each pixel location transferred upon demand to a common bus. In a preferred embodiment, exposure time of the imaging array is controlled using a feedback loop. One or more exposure control pixels are positioned adjacent to or within the imaging array and receive light along with the imaging array. The charge of the exposure control pixel or pixels is measured against a threshold level, and the amount of time taken to reach the threshold level determines the time exposure of the pixels of the imaging array. CMOS signal processing circuitry is employed which, in combination with the exposure control circuitry, minimizes time-to-read over a large range of light levels, while performing spatially optimal filtering. Clocking cycles and control signals are time-adjusted in accordance with the varying output frequency of the imaging array so as to provide invariant frequency response by the signal processing circuitry. A multi-dimensional CMOS imaging array is also provided having simultaneous pixel exposure with non-destructive readout of the pixel contents.

24 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 18. Document ID: US 6195676 B1

L5: Entry 18 of 60 File: USPT Feb 27, 2001

US-PAT-NO: 6195676
DOCUMENT-IDENTIFIER: US 6195676 B1

TITLE: Method and apparatus for user side scheduling in a multiprocessor operating system program that implements distributive scheduling of processes

DATE-ISSUED: February 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Spix; George A.	Eau Claire	WI		
Wengelski; Diane M.	Eau Claire	WI		
Hawkinson; Stuart W.	Eau Claire	WI		
Johnson; Mark D.	Eau Claire	WI		
Burke; Jeremiah D.	Eau Claire	WI		
Thompson; Keith J.	Eau Claire	WI		
Gaertner; Gregory G.	Eau Claire	WI		
Brussino; Giacomo G.	Eau Claire	WI		
Hessel; Richard E.	Altoona	WI		
Barkai; David M.	Eau Claire	WI		
Chen; Steve S.	Chippewa Falls	WI		
Oslon; Steven G.	Chippewa Falls	WI		
Strout, II; Robert E.	Livermore	CA		
Masamitsu; Jon A.	Livermore	CA		
Cox; David M.	Livermore	CA		
O'Gara; Linda J.	Livermore	CA		
O'Hair; Kelly T.	Livermore	CA		
Seberger; David A.	Livermore	CA		
Rasbold; James C.	Livermore	CA		
Cramer; Timothy J.	Pleasanton	CA		
Van Dyke; Don A.	Pleasanton	CA		
Chandramouli; Ashok	Fremont	CA		

US-CL-CURRENT: 718/107

ABSTRACT:

An integrated software architecture for a highly parallel multiprocessor system having multiple tightly-coupled processors that share a common memory efficiently controls the interface with and execution of programs on such a multiprocessor system. The software architecture combines a symmetrically integrated multithreaded operating system and an integrated parallel user environment. The operating system distributively implements an anarchy-based scheduling model for the scheduling of processes and resources by allowing each processor to access a single image of the operating system stored in the common memory that operates on a common set of operating system shared resources. The user environment provides a common visual representation for a plurality of program development tools that provide compilation, execution and debugging capabilities for multithreaded user programs and assumes parallelism as the standard mode of operation.

6 Claims, 59 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 55

☐ 19. Document ID: US 6176429 B1

L5: Entry 19 of 60 File: USPT Jan 23, 2001

US-PAT-NO: 6176429
DOCUMENT-IDENTIFIER: US 6176429 B1

TITLE: Optical reader with selectable processing characteristics for reading data in multiple formats

DATE-ISSUED: January 23, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reddersen; Brad R.	Eugene	OR		
Bremer; Edward C.	Rochester	NY		
La; Chay K.	Rochester	NY		
Deloge; Stephen P.	Rochester	NY		
Boyd; Raymond J.	Bloomfield	NY		
Cooper; Shane P.	Walworth	NY		
Zaverukha; Ilya	Penfield	NY		

US-CL-CURRENT: 235/462.25; 235/462.28

ABSTRACT:

A multi-function optical reader comprises an photosensor, such as a charge-device (CCD), and signal conditioning and processing circuitry including separate channels for handling data in different formats. A bar code processing channel digitizes the scan signal according to light and dark features using a first-derivative technique, and an OMR processing channel uses an adaptive threshold to adapt to different light conditions and provide a boundary line for digitizing light and dark features of the target scan line. A feature measurement circuit measures the widths of the light and dark regions as derived by the separate processing channels, and provides the feature measurements to a decoding system or host terminal processor. The scan rate of the optical reader can be adjusted according to the data format to be read or the level of ambient light, to avoid saturation. The optical reader can provide multiple depth-of-field zones, both internal and external to an optical reader housing. The optical reader may provide for image capture and optical character recognition.

32 Claims, 49 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 38

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 20. Document ID: US 6173894 B1

L5: Entry 20 of 60 File: USPT Jan 16, 2001

US-PAT-NO: 6173894
DOCUMENT-IDENTIFIER: US 6173894 B1

TITLE: Optical reader with addressable pixels

DATE-ISSUED: January 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olmstead; Bryan L.	Eugene	OR		
Colley; James E.	Eugene	OR		

US-CL-CURRENT: 235/462.17; 235/462.01

ABSTRACT:

An optical or symbol reader including CMOS circuitry preferably integrated on a single chip. A CMOS optical reader chip comprises a CMOS imaging array having a plurality of pixels each with a dedicated pixel-site circuit. Charge is accumulated at each pixel location transferred upon demand to a common bus. In a preferred embodiment, exposure time of the imaging array is controlled using a feedback loop. One or more exposure control pixels are positioned adjacent to or within the imaging array and receive light along with the imaging array. The charge of the exposure control pixel or pixels is measured against a threshold level, and the amount of time taken to reach the threshold level determines the time exposure of the pixels of the imaging array. CMOS signal processing circuitry is employed which, in combination with the exposure control circuitry, minimizes time-to-read over a large range of light levels, while performing spatially optimal filtering. Clocking cycles and control signals are time-adjusted in accordance with the varying output frequency of the imaging array so as to provide invariant frequency response by the signal processing circuitry. A multi-dimensional CMOS imaging array is also provided having simultaneous pixel exposure with non-destructive readout of the pixel contents.

15 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 21. Document ID: US 6157231 A

L5: Entry 21 of 60 File: USPT Dec 5, 2000

US-PAT-NO: 6157231
DOCUMENT-IDENTIFIER: US 6157231 A

TITLE: Delay stabilization system for an integrated circuit

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wasson; Timothy M.	Portland	OR		

US-CL-CURRENT: 327/156; 327/158, 327/161

ABSTRACT:

A system for stabilizing a delay through a signal path of an integrated circuit (IC) includes an oscillator for producing a periodic first reference signal, a delay circuit for delaying the first reference signal to produce a periodic second reference signal, and a loop controller for adjusting the magnitude of the IC's power supply so as to maintain a constant phase difference between the first and second reference signals. By adjusting the power supply magnitude, the loop controller also stabilizes signal path delays through logic circuits implemented in the IC. The oscillator is formed by a logic gate implemented in the IC and a passive delay line feeding the logic gate's output back to its input. The delay of the delay circuit is programmably adjustable to allow for adjustment of the signal path delay through the IC.

17 Claims, 3 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

☐ 22. Document ID: US 6155488 A

L5: Entry 22 of 60 File: USPT Dec 5, 2000

US-PAT-NO: 6155488
DOCUMENT-IDENTIFIER: US 6155488 A

TITLE: Optical reader with adaptive exposure control

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olmstead; Bryan L.	Eugene	OR		
Colley; James E.	Eugene	OR		

US-CL-CURRENT: 235/440; 235/462.01

ABSTRACT:

An optical or symbol reader including CMOS circuitry preferably integrated on a single chip. A CMOS optical reader chip comprises a CMOS imaging array having a plurality of pixels each with a dedicated pixel-site circuit. Charge is accumulated at each pixel location transferred upon demand to a common bus. In a preferred embodiment, exposure time of the imaging array is controlled using a feedback loop. One or more exposure control pixels are positioned adjacent to or within the imaging array and receive light along with the imaging array. The charge of the

exposure control pixel or pixels is measured against a threshold level, and the amount of time taken to reach the threshold level determines the time exposure of the pixels of the imaging array. CMOS signal processing circuitry is employed which, in combination with the exposure control circuitry, minimizes time-to-read over a large range of light levels, while performing spatially optimal filtering. Clocking cycles and control signals are time-adjusted in accordance with the varying output frequency of the imaging array so as to provide invariant frequency response by the signal processing circuitry. A multi-dimensional CMOS imaging array is also provided having simultaneous pixel exposure with non-destructive readout of the pixel contents.

22 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 23. Document ID: US 6152368 A

L5: Entry 23 of 60 File: USPT Nov 28, 2000

US-PAT-NO: 6152368
DOCUMENT-IDENTIFIER: US 6152368 A
**** See image for Certificate of Correction ****

TITLE: Optical reader with addressable pixels

DATE-ISSUED: November 28, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olmstead; Bryan L.	Eugene	OR		
Colley; James E.	Eugene	OR		

US-CL-CURRENT: 235/454; 235/462.41, 235/470

ABSTRACT:

An optical or symbol reader including CMOS circuitry preferably integrated on a single chip. A CMOS optical reader chip comprises a CMOS imaging array having a plurality of pixels each with a dedicated pixel-site circuit. Charge is accumulated at each pixel location transferred upon demand to a common bus. In a preferred embodiment, exposure time of the imaging array is controlled using a feedback loop. One or more exposure control pixels are positioned adjacent to or within the imaging array and receive light along with the imaging array. The charge of the exposure control pixel or pixels is measured against a threshold level, and the amount of time taken to reach the threshold level determines the time exposure of the pixels of the imaging array. CMOS signal processing circuitry is employed which, in combination with the exposure control circuitry, minimizes time-to-read over a large range of light levels, while performing spatially optimal filtering. Clocking cycles and control signals are time-adjusted in accordance with the varying output frequency of the imaging array so as to provide invariant frequency response by the signal processing circuitry. A multi-dimensional CMOS imaging array is also provided having simultaneous pixel exposure with non-destructive readout of

the pixel contents.

11 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 24. Document ID: US 6141169 A

L5: Entry 24 of 60 File: USPT Oct 31, 2000

US-PAT-NO: 6141169
DOCUMENT-IDENTIFIER: US 6141169 A

TITLE: System and method for control of low frequency input levels to an amplifier and compensation of input offsets of the amplifier

DATE-ISSUED: October 31, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pietruszynski; David M.	Austin	TX		
Hein; Jerrell P.	Driftwood	TX		
Bliss; William G.	Thornton	CO		
Feyh; German S.	Boulder	CO		

US-CL-CURRENT: 360/67; 330/260

ABSTRACT:

A system and method for an amplifier control circuit is provided which does not require the use of a large off-chip or on-chip capacitor for achieving a low frequency coupling corner, while still effectively allowing AC coupling the data detection circuit. In addition, the input offset voltage to the amplifier may be compensated and the inherent random low frequency input voltages provided to the amplifier may be controlled or canceled.

Further, the amplifier control circuitry includes a freeze capability which allows the control circuitry to halt all updates to the input offset/low frequency control circuit when the voltage input signal is interrupted. In addition low frequency control and offset compensation updates may be performed without causing large output signal glitches so that the integrity of the received signal will not be compromised. In a preferred embodiment the system and method may be utilized for data detection circuits utilized in conjunction with optical disks.

14 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

☐ 25. Document ID: US 6101108 A

L5: Entry 25 of 60 File: USPT Aug 8, 2000

US-PAT-NO: 6101108
DOCUMENT-IDENTIFIER: US 6101108 A

TITLE: Regulated input current, regulated output voltage power converter

DATE-ISSUED: August 8, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wittenbreder, Jr.; Ernest Henry	Flagstaff	AZ		

US-CL-CURRENT: 363/65; 323/222, 323/239, 363/127, 363/89

ABSTRACT:

The power conversion system of this invention achieves precisely regulated input current and precisely regulated output voltage in a two step process whereby one power converter sub-system (141) provides input current regulation and a second power converter sub-system (158) provides output voltage regulation. The two converter sub-systems are arranged so that the second power converter sub-system (158) is powered by the first power converter sub-system (141) and the output of the second power converter sub-system (158) is placed in series with an output of the first power converter sub-system (141) to form the system output so that the load voltage is the sum of the two outputs placed in series. With this arrangement only a small fraction of the load power needs to be processed by the second power converter sub-system (158) which yields higher system efficiency and smaller system size, weight, and cost.

3 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 9

☐ 26. Document ID: US 6069866 A

L5: Entry 26 of 60 File: USPT May 30, 2000

US-PAT-NO: 6069866
DOCUMENT-IDENTIFIER: US 6069866 A
**** See image for Certificate of Correction ****

TITLE: System and method for coarse gain control of wide band amplifiers

DATE-ISSUED: May 30, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY

Pietruszynski; David M.	Austin	TX
Tesu; Ion Constantin	Austin	TX

US-CL-CURRENT: 369/124.11; 330/254

ABSTRACT:

A system and method for a data detection circuit is provided in which separate coarse gain amplifiers and fine gain amplifiers are utilized. The coarse gain amplifiers may include drain switching of transistors in order to modify the amplifier gain. More particularly, drain switching may be utilized to selectively switch in and out different differential input transistor pairs and/or different current sources. In this manner the gain of the amplifier may be adjusted to one of a variety of different coarse gain control levels. The coarse gain control provided allows for gain adjustments without significantly decreasing the bandwidth of the amplifier. In a preferred embodiment the system and method may be utilized for data detection circuits utilized in conjunction with optical disks.

26 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

☐ 27. Document ID: US 5903350 A

L5: Entry 27 of 60 File: USPT May 11, 1999

US-PAT-NO: 5903350
DOCUMENT-IDENTIFIER: US 5903350 A

TITLE: Demodulator and method useful for multiplexed optical sensors

DATE-ISSUED: May 11, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bush; Ira Jeffery	Los Angeles	CA		
Cekorich; Allen Curtis	Walnut Creek	CA		

US-CL-CURRENT: 356/478; 329/346

ABSTRACT:

An apparatus and method is presented to provide wide dynamic range measurements of the input phase to an interferometer using a phase generated carrier especially useful utilizing time multiplexing to demodulate a series of interferometers. A modulation drive output is provided by the invention and maintained under operation at the optimum amplitude by an internal feedback loop. The resulting highly stable system can be fabricated from an analog to digital converter, a digital signal processor, and a digital to analog converter making low cost open loop demodulators a reality.

25 Claims, 50 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 28. Document ID: US 5869248 A

L5: Entry 28 of 60 File: USPT Feb 9, 1999

US-PAT-NO: 5869248
DOCUMENT-IDENTIFIER: US 5869248 A

TITLE: Targeted cleavage of RNA using ribonuclease P targeting and cleavage sequences

DATE-ISSUED: February 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yuan; Yan	New Haven	CT		
Guerrier-Takada; Cecilia	New Haven	CT		
Altman; Sidney	Hamden	CT		
Liu; Fenyong	New Haven	CT		

US-CL-CURRENT: 435/6; 536/23.2

ABSTRACT:

It has been discovered that any RNA can be targeted for cleavage by RNase P from prokaryotic or eukaryotic cells using a suitably designed oligonucleotide ("external guide sequence", or EGS) to form a hybrid with the target RNA, thereby creating a substrate for cleavage by RNase P in vitro. The EGS hydrogen bonds to the targeted RNA to form a partial tRNA like structure including the aminoacyl acceptor stem, the T stem and loop, and part of the D stem. An EGS can be modified both by changes in sequence and by chemical modifications to the nucleotides. The EGS can be a separate molecule or can be combined with an RNase P catalytic RNA sequence to form a single oligonucleotide molecule ("RNase P internal guide sequence" or RIGS). Methods are also disclosed to randomly select and to express a suitable EGS or RIGS in vivo to make a selected RNA a target for cleavage by a host cell RNase P or introduced RIGS, thus preventing expression of the function of the target RNA. The methods and compositions should be useful to prevent the expression of disease- or disorder-causing genes in vivo.

30 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 29. Document ID: US 5867341 A

L5: Entry 29 of 60 File: USPT Feb 2, 1999

US-PAT-NO: 5867341
DOCUMENT-IDENTIFIER: US 5867341 A

TITLE: Disc drive system using multiple pairs of embedded servo bursts

DATE-ISSUED: February 2, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Volz; LeRoy A.	Northridge	CA		
Manz; Stephen R.	Canoga Park	CA		
Hurst; Raymond E.	Palmdale	CA		

US-CL-CURRENT: 360/77.08; 360/77.02

ABSTRACT:

A method and apparatus determining head position of a data transducer head relative to a selected one track of a multiplicity of concentric tracks within a magnetic/disc drive is provided. At least one prerecorded servo sector within a data track includes four time staggered servo bursts. The first pair and second pair of servo bursts are radially offset from each other by generally a burst width such that an edge from each of the pair are substantially co-linear in forming a track null. The first pair is radially offset from the second pair by one-half of the burst width. The first pair is read to determine a first relative amplitude therebetween, and the second pair is read to determine a second relative amplitude therebetween. Additionally, the radially offset and time staggered servo bursts prerecorded on the servo sector can be of varying width and numbered to create the plurality of track nulls within a data track about which the head can be positioned.

12 Claims, 15 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 30. Document ID: US 5758164 A

L5: Entry 30 of 60 File: USPT May 26, 1998

US-PAT-NO: 5758164
DOCUMENT-IDENTIFIER: US 5758164 A

TITLE: Method and system for processing language

DATE-ISSUED: May 26, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Inoue; Masaharu	Tokyo			JP

US-CL-CURRENT: 717/158; 717/146, 717/156, 717/159

ABSTRACT:

In a language processing system for translating a source program into a machine program, a range of the source program to be optimized is discriminated during parsing to generate an optimization enabling and disabling code to be inserted in an intermediate code resulting from parsing. An optimization process for the intermediate code is performed only for a range, in which optimization can be performed, determined on the basis of the optimization enabling and disabling code.

16 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

☐ 31. Document ID: US 5728521 A

L5: Entry 31 of 60 File: USPT Mar 17, 1998

US-PAT-NO: 5728521
DOCUMENT-IDENTIFIER: US 5728521 A

TITLE: Targeted cleavage of RNA using eukaryotic ribonuclease P and external guide sequence

DATE-ISSUED: March 17, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yuan; Yan	New Haven	CT		
Guerrier-Takada; Cecilia	New Haven	CT		
Altman; Sidney	Hamden	CT		
Liu; Fenyong	New Haven	CT		

US-CL-CURRENT: 435/6; 435/91.2

ABSTRACT:

It has been discovered that any RNA can be targeted for cleavage by RNAase P from eukaryotic cells, for example, human RNAase P, using a suitably designed oligoribonucleotide ("external guide sequence", or EGS) to form a hybrid with the target RNA, thereby creating a substrate for cleavage by RNAase P in vitro. The EGS hydrogen bonds to the targeted RNA to form a partial tRNA like structure including the aminoacyl acceptor stem, the T stem and loop, and part of the D stem. The most efficient EGS with human RNAase P is the EGS in which the anticodon stem and loop was deleted. Modifications can also be made within the T-loop. Methods are also disclosed to randomly select and to express a suitable EGS in vivo to make a

selected RNA a target for cleavage by the host cell RNAase P, thus preventing expression of the function of the target RNA. The methods and compositions should be useful to prevent the expression of disease-causing genes in vivo.

7 Claims, 15 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 32. Document ID: US 5723517 A

L5: Entry 32 of 60 File: USPT Mar 3, 1998

US-PAT-NO: 5723517
DOCUMENT-IDENTIFIER: US 5723517 A

TITLE: System for controlling the color of compounded polymer(s) using in-process color measurements

DATE-ISSUED: March 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Campo; Peter John	Niskayuna	NY		
Houpt; Paul Kenneth	Schenectady	NY		

US-CL-CURRENT: 523/303; 137/93, 366/152.1, 425/135, 425/145, 425/169, 700/266, 700/95

ABSTRACT:

A system for controlling the color of compounded polymer(s) comprises: a compounder for mixing the constituents of the compounded polymer(s) to produce a substantially homogeneous mixture; a sensor for measuring the color of the substantially homogeneous mixture at predetermined intervals; a colorant additive feeder, responsive to a controller, for providing the colorant additive(s) to the mixture at substantially predetermined colorant additive addition rates; and a controller, responsive to the sensor, for controlling the colorant additive addition rate(s) of the feeder.

10 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

☐ 33. Document ID: US 5677153 A

L5: Entry 33 of 60 File: USPT Oct 14, 1997

US-PAT-NO: 5677153
DOCUMENT-IDENTIFIER: US 5677153 A
**** See image for Certificate of Correction ****

TITLE: Methods for modifying DNA and for detecting effects of such modification on interaction of encoded modified polypeptides with target substrates

DATE-ISSUED: October 14, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Botstein; David	Belmont	CA		
Palzkill; Timothy	Union City	CA		

US-CL-CURRENT: 435/91.4; 435/91.2, 435/91.41, 435/91.42

ABSTRACT:

The invention relates to methods and mutation linkers to modify DNA, to methods for producing libraries containing a multiplicity of modified DNA, and to methods for using such libraries for screening modified proteins encoded by such DNA. The DNA targeted for modification typically encodes a polypeptide such as an enzyme. The libraries are used to determine the effect of such modification or the interaction of the modified polypeptides with a target. In preferred embodiments, the invention relates to methods for making and using libraries containing DNA encoding modified antibiotic hydrolases to screen antibiotics against one or more of the modified antibiotic hydrolases produced by such libraries. Susceptibility or lack of susceptibility of an antibiotic to neutralization provides an indication of whether wild-type antibiotic hydrolases are likely to mutate to confer resistance to the antibiotic.

40 Claims, 55 Drawing figures
Exemplary Claim Number: 2
Number of Drawing Sheets: 23

☐ 34. Document ID: US 5624824 A

L5: Entry 34 of 60 File: USPT Apr 29, 1997

US-PAT-NO: 5624824
DOCUMENT-IDENTIFIER: US 5624824 A

TITLE: Targeted cleavage of RNA using eukaryotic ribonuclease P and external guide sequence

DATE-ISSUED: April 29, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yuan; Yan	New Haven	CT		

Guerrier-Takada; Cecilia	New Haven	CT
Altman; Sidney	Hamden	CT
Liu; Fenyong	New Haven	CT

US-CL-CURRENT: 435/91.2; 514/44, 536/23.1

ABSTRACT:

It has been discovered that any RNA can be targeted for cleavage by RNAase P from eukaryotic cells, for example, human RNAase P, using a suitably designed oligoribonucleotide ("external guide sequence", or EGS) to form a hybrid with the target RNA, thereby creating a substrate for cleavage by RNAase P in vitro. The EGS hydrogen bonds to the targeted RNA to form a partial tRNA like structure including the aminoacyl acceptor stem, the T stem and loop, and part of the D stem. The most efficient EGS with human RNAase P is the EGS in which the anticodon stem and loop was deleted. Modifications can also be made within the T-loop. Methods are also disclosed to randomly select and to express a suitable EGS in vivo to make a selected RNA a target for cleavage by the host cell RNAase P, thus preventing expression of the function of the target RNA. The methods and compositions should be useful to prevent the expression of disease-causing genes in vivo.

17 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 35. Document ID: US 5559173 A

L5: Entry 35 of 60 File: USPT Sep 24, 1996

US-PAT-NO: 5559173
DOCUMENT-IDENTIFIER: US 5559173 A

TITLE: System for controlling the color of compounded polymer(s) using in-process color measurements

DATE-ISSUED: September 24, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Campo; Peter J.	Niskayuna	NY		
Houpt; Paul K.	Schenectady	NY		

US-CL-CURRENT: 523/303; 137/93, 356/409, 356/412, 356/414, 356/425, 366/152.1

ABSTRACT:

A system for controlling the color of compounded polymer(s) comprises: a compounder for mixing the constituents of the compounded polymer(s) to produce a substantially homogeneous mixture; a sensor for measuring the color of the substantially homogeneous mixture at predetermined intervals; a colorant additive feeder, responsive to a controller, for providing the colorant additive(s) to the mixture

at substantially predetermined colorant additive addition rates; and a controller, responsive to the sensor, for controlling the colorant additive addition rate(s) of the feeder.

10 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

☐ 36. Document ID: US 5535391 A

L5: Entry 36 of 60 File: USPT Jul 9, 1996

US-PAT-NO: 5535391
DOCUMENT-IDENTIFIER: US 5535391 A

TITLE: System and methods for optimizing object-oriented compilations

DATE-ISSUED: July 9, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hejlsberg; Anders	Aptos	CA		
Stock; Jeffrey	Scotts Valley	CA		
Kukol; Peter	Aptos	CA		
Shtaygrud; Alex	San Jose	CA		

US-CL-CURRENT: 717/140; 717/165

ABSTRACT:

An object-oriented development system of the present invention includes a language compiler having an optimizer for generating computer applications with improved speed and size. C++ optimization methods of the present invention are described, including virtual function and base optimization, using thunks for virtual member pointers, and passing classes by value. An object-oriented calling convention of the present invention, which affords rapid and efficient access to data and methods of objects, is also described.

19 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 37. Document ID: US 5490057 A

L5: Entry 37 of 60 File: USPT Feb 6, 1996

US-PAT-NO: 5490057
DOCUMENT-IDENTIFIER: US 5490057 A
** See image for Certificate of Correction **

TITLE: Feedback control system having predictable open-loop gain

DATE-ISSUED: February 6, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Vinciarelli; Patrizio	Boston	MA		
Bufano; Louis A.	Tewksbury	MA		

US-CL-CURRENT: 700/37; 363/16, 702/109, 702/126

ABSTRACT:

A closed-loop feedback system has first and second gain elements. The first gain element has a transfer function such that Xd=Kg * (Xcont).sup.z, where Xcont is a control variable input signal of the first gain element, Xd is a controlled variable output signal of the first gain element, and Kg and z are independent of Xcont. The second gain element has a transfer function h1 such that Xcont=h1(Xe) where Xe is a control variable input signal of the second gain element and Xcont is a controlled variable output signal of the second gain element. The function h1 is of a form which satisfies [1/h1(Xe)]*[.delta.h1(Xe)/.delta.Xe]=Ke, where Ke is independent of Xe.

51 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 14

☐ 38. Document ID: US 5481708 A

L5: Entry 38 of 60 File: USPT Jan 2, 1996

US-PAT-NO: 5481708
DOCUMENT-IDENTIFIER: US 5481708 A

TITLE: System and methods for optimizing object-oriented compilations

DATE-ISSUED: January 2, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kukol; Peter	Aptos	CA		

US-CL-CURRENT: 717/155; 717/165

ABSTRACT:

An object-oriented development system of the present invention includes a language compiler having an optimizer for generating computer applications with improved speed and size. C++ optimization methods of the present invention are described, including virtual function and base optimization, using thunks for virtual member pointers, and passing classes by value. An object-oriented calling convention of the present invention, which affords rapid and efficient access to data and methods of objects, is also described.

13 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

☐ 39. Document ID: US 5394322 A

L5: Entry 39 of 60 File: USPT Feb 28, 1995

US-PAT-NO: 5394322
DOCUMENT-IDENTIFIER: US 5394322 A

TITLE: Self-tuning controller that extracts process model characteristics

DATE-ISSUED: February 28, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hansen; Peter D.	Wellesley Hills	MA		

US-CL-CURRENT: 700/37; 700/32, 700/38, 700/42

ABSTRACT:

An apparatus and method for process control that extracts information from a process for developing a model of the process that is used to design system control. The apparatus includes means for selecting a process model form that has two or more selectable parameters. The apparatus also includes means for deliberately disturbing a process that is in open-loop operation and that is in a substantially settled state and further includes means for measuring the process response. The apparatus selects parameters for the process model form according to a function of the measured process response. In this way a complete model of the process is identified. The apparatus self-tunes by directly calculating new control parameters according to a function of the identified open-loop process model and a preselected target behavior.

24 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 40. Document ID: US 5230050 A

L5: Entry 40 of 60 File: USPT Jul 20, 1993

US-PAT-NO: 5230050
DOCUMENT-IDENTIFIER: US 5230050 A

TITLE: Method of recompiling a program by using result of previous compilation

DATE-ISSUED: July 20, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Iitsuka; Takayoshi	Hachioji			JP
Kikuchi; Sumio	Machida			JP

US-CL-CURRENT: 717/145; 717/146, 717/155

ABSTRACT:

A program compiling method in which a procedure being compiled is split into a plurality of units referred to as segments, whereon optimization is carried out for each of the segments. Upon recompilation of the procedure, optimization of the procedure is redone not for the whole of the procedure but executed only on the segments which are affected by modification, while for the segments insusceptible to the influence of modification, object program obtained by the compilation or the intermediate codes available in the course of the optimization are reused. At several stages of optimization, intermediate results of the optimization are recorded, wherein upon recompilation, the intermediate results of optimization obtained in the preceding compilation are made use of up to the stage where no influence of modification makes appearance. The amount of processing involved in the optimization can thus be reduced even when the object program can not be utilized. In a mode for carrying out the invention, not only the interim results of optimization but also the contents of optimization executed are recorded. Upon recompilation, those of the optimization processings executed in the preceding compilation which are to be executed again can be performed rapidly by making use of the contents stored. The time taken for the execution of optimization processing to be re-executed can be reduced significantly.

20 Claims, 32 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 30

☐ 41. Document ID: US 5179702 A

L5: Entry 41 of 60 File: USPT Jan 12, 1993

US-PAT-NO: 5179702
DOCUMENT-IDENTIFIER: US 5179702 A

TITLE: System and method for controlling a highly parallel multiprocessor using an anarchy based scheduler for parallel execution thread scheduling

DATE-ISSUED: January 12, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Spix; George A.	Eau Claire	WI		
Wengelski; Diane M.	Eau Claire	WI		
Hawkinson; Stuart W.	Eau Claire	WI		
Johnson; Mark D.	Eau Claire	WI		
Burke; Jeremiah D.	Eau Claire	WI		
Thompson; Keith J.	Eau Claire	WI		
Gaertner; Gregory G.	Eau Claire	WI		
Brussino; Giacomo G.	Eau Claire	WI		
Hessel; Richard E.	Altoona	WI		
Barkai; David M.	Eau Claire	WI		
Chen; Steve S.	Chippewa Falls	WI		
Oslon; Steven G.	Chippewa Falls	WI		
Strout, II; Robert E.	Livermore	CA		
Masamitsu; Jon A.	Livermore	CA		
Cox; David M.	Livermore	CA		
O'Gara; Linda J.	Livermore	CA		
O'Hair; Kelly T.	Livermore	CA		
Seberger; David A.	Livermore	CA		
Rasbold; James C.	Livermore	CA		
Cramer; Timothy J.	Pleasanton	CA		
Van Dyke; Don A.	Pleasanton	CA		
Chandramouli; Ashok	Fremont	CA		

US-CL-CURRENT: 718/102; 717/124, 717/146, 717/151, 718/104, 718/106

ABSTRACT:

An integrated software architecture for a highly parallel multiprocessor system having multiple tightly-coupled processors that share a common memory efficiently controls the interface with and execution of programs on such a multiprocessor system. The software architecture combines a symmetrically integrated multithreaded operating system and an integrated parallel user environment. The operating system distributively implements an anarchy-based scheduling model for the scheduling of processes and resources by allowing each processor to access a single image of the operating system stored in the common memory that operates on a common set of operating system shared resources. The user environment provides a common visual representation for a plurality of program development tools that provide compilation, execution and debugging capabilities for multithreaded user programs and assumes parallelism as the standard mode of operation.

12 Claims, 60 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 53

☐ 42. Document ID: US 5175856 A

L5: Entry 42 of 60 File: USPT Dec 29, 1992

US-PAT-NO: 5175856
DOCUMENT-IDENTIFIER: US 5175856 A
**** See image for Certificate of Correction ****

TITLE: Computer with integrated hierarchical representation (IHR) of program wherein IHR file is available for debugging and optimizing during target execution

DATE-ISSUED: December 29, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Van Dyke; Don A.	Pleasanton	CA		
Cramer; Timothy J.	Pleasanton	CA		
Rasbold; James C.	Livermore	CA		
O'Hair; Kelly T.	Livermore	CA		
Cox; David M.	Livermore	CA		
Seberger; David A.	Livermore	CA		
O'Gara; Linda J.	Livermore	CA		
Masamitsu; Jon A.	Livermore	CA		
Strout, II; Robert E.	Livermore	CA		
Chandramouli; Ashok	Fremont	CA		

US-CL-CURRENT: 717/151; 717/124, 717/159

ABSTRACT:

A modular compilation system that utilizes a fully integrated hierarchical representation as a common intermediate representation to compile source code programs written in one or more procedural programming languages into an executable object code file. The structure of the integrated common intermediate representation supports machine-independent optimizations, as well as machine-dependent optimizations, and also supports source-level debugging of the executable object code file. The integrated hierarchical representation (IHR) is language independent and is shared by all of the components of the software development system, including the debugger.

18 Claims, 16 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 16

☐ 43. Document ID: US 5170299 A

L5: Entry 43 of 60 File: USPT Dec 8, 1992

US-PAT-NO: 5170299
DOCUMENT-IDENTIFIER: US 5170299 A

TITLE: Edge servo for disk drive head positioner

DATE-ISSUED: December 8, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Moon; Ronald R.	Los Gatos	CA		

US-CL-CURRENT: 360/77.08; 360/51, 360/78.04, 360/78.14

ABSTRACT:

A method for determining the position of a data transducer head within one data track of a rotating data storage disk within a disk drive includes the steps of:

providing at least one prerecorded servo sector within the data track, the servo sector including first occurring servo burst having one longitudinal burst edge located substantially congruent with a centerline of the one track, and having another longitudinal burst edge located substantially congruent with a centerline of a second track adjacent to the one track, and second servo burst having longitudinal burst edges substantially congruent with the track boundaries of the one track.

detecting the presence of the sector as it passes by the data transducer head,

sampling with the data transducer head and holding peak amplitude of the first servo burst,

sampling with the data transducer head and holding peak amplitude of the second servo burst,

comparing held first burst amplitude with a predetermined value to determine if the data transducer head has passed over a linear edge portion thereof, and if so, determining from the held first burst amplitude the position; and if not, determining from the held second burst amplitude the position of the data transducer head relative to the one track.

27 Claims, 14 Drawing figures
Exemplary Claim Number: 19
Number of Drawing Sheets: 9

☐ 44. Document ID: US 4933620 A

L5: Entry 44 of 60 File: USPT Jun 12, 1990

US-PAT-NO: 4933620
DOCUMENT-IDENTIFIER: US 4933620 A
**** See image for Certificate of Correction ****

TITLE: Control system for low speed switched reluctance motor

DATE-ISSUED: June 12, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
MacMinn; Stephen R.	Schenectady	NY		
Sember; James W.	Roanoke	VA		

US-CL-CURRENT: 318/696; 318/685, 318/701

ABSTRACT:

A method and apparatus for improving the operation of a switched reluctance motor at low speed incorporates an advance angle regulator which regulates the firing angle of current pulses to the switched reluctance motor so that over a wide range of speeds and levels for direct current source voltages, the winding current reaches a commanded set point at a commanded angle. The advance angle regulator may comprise a closed loop regulator which includes apparatus for detecting the actual angular position at which motor current reaches a commanded level and adjusts the turn-on angle to shift the angle at which current reaches its desired level to a desired angle. The regulator incorporates a feedforward portion and an integral portion. The feedforward portion is utilized primarily to accommodate situations in which there is no current feedback. The integral portion provides the primary regulation when current is regulated to its desired value. The regulator causes the torque versus current command to have a transfer function which does not depend upon speed or DC source voltage over a wide range of speed, voltage and torque.

14 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

☐ 45. Document ID: US 4926105 A

L5: Entry 45 of 60 File: USPT May 15, 1990

US-PAT-NO: 4926105
DOCUMENT-IDENTIFIER: US 4926105 A

TITLE: Method of induction motor control and electric drive realizing this method

DATE-ISSUED: May 15, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mischenko; Vladislav A.	Moscow, Orekhovy bulvar			SU
Mischenko; Natalya I.	Moscow, Orekhovy bulvar			SU

US-CL-CURRENT: 318/800; 318/805

ABSTRACT:

Method of induction motor vector control in Cartesian and polar coordinates, whereby control of the rotor speed, induction motor torque, as well as dynamic, power, and thermal processes, which is interconnected with control of the rotor

flux linkage amplitude and phase as functions of the desired induction motor torque, is achieved in an electric drive by synchronizing the stator current control by a controlled synchronization frequency by means of three control inputs, one control input is used to control the synchronization frequency and phase as functions of the desired rotor torque and speed; two other control inputs are used to control the amplitudes of ortho-phasal and current phase to a phase angle equal to the ratio of the ortho-phasal and co-phasal and ortho-phasal currents as functions of the desired induction motor torque, the actual desired amplitude of the rotor flux linkage, and magnetizing characteristic of the induction motor, while the amplitudes of the ortho-phasal and co-phasal currents is kept mostly equal, the synchronization phase being additionally controlled as a function of the induction motor temperature. An apparatus is described to carry out the method.

6 Claims, 27 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

☐ 46. Document ID: US 4847603 A

L5: Entry 46 of 60 File: USPT Jul 11, 1989

US-PAT-NO: 4847603
DOCUMENT-IDENTIFIER: US 4847603 A

TITLE: Automatic closed loop scaling and drift correcting system and method particularly for aircraft head up displays

DATE-ISSUED: July 11, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blanchard; Clark E.	Kentwood	MI	49508	

US-CL-CURRENT: 345/7; 340/980, 348/169, 359/630

ABSTRACT:

A display system and method, especially for use in an aircraft head up display system, for maintaining an optical image in a predetermined position on a light emitting screen. The system has a beam type image generator controlled by an operating circuit. A controlled beam scans both a central display region and marginal regions of the screen. The marginal regions have beam sensors and the beam is controlled by a sequence of plural coordinate commands in accordance with a plural coordinate search pattern restricted to the marginal regions and in the vicinity of the beam sensors. Signals resulting therefrom are utilized to eliminate beam deflection errors.

45 Claims, 42 Drawing figures
Exemplary Claim Number: 36
Number of Drawing Sheets: 27

☐ 47. Document ID: US 4600906 A

L5: Entry 47 of 60 File: USPT Jul 15, 1986

US-PAT-NO: 4600906
DOCUMENT-IDENTIFIER: US 4600906 A
**** See image for Certificate of Correction ****

TITLE: Magnetically tuned resonant circuit wherein magnetic field is provided by a biased conductor on the circuit support structure

DATE-ISSUED: July 15, 1986

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blight; Ronald E.	Framingham	MA		

US-CL-CURRENT: 333/205; 333/235, 333/24.1, 333/246

ABSTRACT:

A magnetically tuned resonant circuit for coupling r.f. energy between input and output coupling circuits thereof in a first mode of operation and isolating such energy between such coupling circuits in a second mode of operation includes a current path circuit provided to selectively change the resonant frequency of the magnetically tuned resonant circuit. In a first embodiment of the current path circuit, a microstrip transmission line used to form one of such coupling circuits, having a pair of planar spaced strip conductor portions adjacent a resonant body, is configured to provide the current path around such body. In the presence of an external magnetic field H.sub.DC, a pulse of current is fed around the current path and in response thereto provides a pulse magnetic field H.sub.DCp in the region of the resonant body. Such field H.sub.DCp either aids or opposes the external magnetic field H.sub.DC and in response thereto shifts a resonant frequency .omega..sub.o of such circuit in accordance with the equation .omega..sub.o =.gamma.(H.sub.DC .+-.H.sub.DCp) where .gamma. is a quantity known as the gyromagnetic ratio. In an alternate embodiment of the circuit, the circuit includes a coil supported on a dielectric substrate to provide the current path, with such coil being disposed adjacent the resonant body. A pulse of current is fed to the coil providing a magnetic field H.sub.DCp, and in the presence of the external magnetic field H.sub.DC, the resonant frequency of such circuit is shifted in accordance with the equation .omega..sub.o =.gamma.(H.sub.DC .+-.H.sub.DCp).

28 Claims, 47 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 48. Document ID: US 4543543 A

L5: Entry 48 of 60 File: USPT Sep 24, 1985

US-PAT-NO: 4543543
DOCUMENT-IDENTIFIER: US 4543543 A

TITLE: Magnetically tuned resonant circuit

DATE-ISSUED: September 24, 1985

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blight; Ronald E.	Framingham	MA		
Schloemann; Ernst F. R. A.	Weston	MA		

US-CL-CURRENT: 333/24.1; 333/204, 333/219.2

ABSTRACT:

A magnetically tuned resonant circuit for selectively coupling radio frequency (r.f.) energy between an input coupling circuit and an output coupling circuit through a resonant body disposed between such coupling circuits. Each coupling circuit includes a plurality of spaced conductors which are arranged to selectively spatially distribute r.f. energy fed thereto in order to provide, in the region where the resonant body is disposed, a magnetic field having a predetermined spatial distribution. Such magnetic field distribution is selected in accordance with characteristics of the resonant body to reduce coupling of unwanted spurious r.f. energy through the magnetically tuned resonant circuit.

Further, a ground plane conductor associated with such coupling circuits has a selected portion thereof removed to provide a void therein, and a portion of the resonant body is disposed within the void provided in the ground plane. The size of the void is selected to increase coupling of r.f. energy through the resonant body, between the input and the output coupling circuits and to reduce coupling of r.f. energy between the body and the ground plane conductor and hence the r.f. energy loss concomitant therewith, without substantially affecting the desired coupling between the coupling circuits.

31 Claims, 47 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

☐ 49. Document ID: US 4521753 A

L5: Entry 49 of 60 File: USPT Jun 4, 1985

US-PAT-NO: 4521753
DOCUMENT-IDENTIFIER: US 4521753 A

TITLE: Tuned resonant circuit utilizing a ferromagnetically coupled interstage line

DATE-ISSUED: June 4, 1985

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Schloemann; Ernst F. R. A.	Weston	MA		

US-CL-CURRENT: 333/204; 333/205, 333/222, 333/24.1

ABSTRACT:

A magnetically tuned resonant circuit for selectively coupling radio frequency (r.f.) energy between an input coupling circuit and an output coupling circuit, dielectrically spaced from the input coupling circuit, through a resonant body disposed therebetween. Each coupling circuit includes a center strip conductor portion dielectrically spaced from a ground plane conductor. Such center strip conductor and ground plane conductor of each coupling circuit are formed on a common surface of a corresponding dielectric. The center strip conductor portions are orthogonally orientated, and have first end portions which are coaxially aligned and terminated with the ground plane. The resonant body is dielectrically supported between each one of such first end portions of such center conductors.

9 Claims, 47 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

☐ 50. Document ID: US 4393921 A

L5: Entry 50 of 60 File: USPT Jul 19, 1983

US-PAT-NO: 4393921
DOCUMENT-IDENTIFIER: US 4393921 A

TITLE: Circuit controlling coolant flow to a non-linear heat exchanger through a non-linear electromechanical valve

DATE-ISSUED: July 19, 1983

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Zbinden; Terry B.	Maple Grove	MN		

US-CL-CURRENT: 165/295; 236/78C, 251/30.04, 318/615

ABSTRACT:

An electronic circuit controls a non-linear electromechanical valve in order that the temperature of approximately 25 gallons of coolant water within a reservoir may be maintained within +2.8.degree. C. to -0.0.degree. C. of a set point temperature from 35.degree. F. to 100.degree. F. The valve regulates circulation of such coolant within a secondary cooling loop incorporating a non-linear heat exchanger for thermal exchange with building water flowing from 20 to 30 gallons per minute. The reservoir coolant water is subject to an essentially instantaneously variable thermal load of 0 to 20 kilowatts due to circulation through logic modules in a primary coolant loop. The electromechanical valve control circuit receives an

external set point temperature signal, and a reservoir coolant temperature signal which is offset in conversion from degrees Kelvin to degrees Centigrade. The electromechanical valve control circuit employs a first feedback signal from a position potentiometer mechanically linked to valve position, which signal is compensated in a breakpoint amplifier to account for valve and heat exchanger non-linearities in the secondary cooling loop. A second feedback signal from a tachometer, mechanically linked to a motor driving the valve through a 1000:1 gear reduction, is utilized to impart circuit stability.

5 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5